Clock KPI System for Better PPA of Complex Clock Design with ClockExplorer

Huada Empyrean Software /
Spreadtrum Communications

ABSTRACT

Under advanced semiconductor technology, the quality of clock will impact the final SoC PPA (Performance, Power, and Area). It may be affected at each stage of the design cycle, especially for the communication chips with huge instance number, large number of clocks, and complicated clock structures. Clock quality control has become the critical problem. Therefore, A KPI system is built based on ClockExplorer platform with scoring functionality, to ensure the clock quality, make clear the responsibility, find and solve the clock design problem.

For Front-end engineers, good clock structure is the foundation of successful CTS. Before signoff RTL codes and sub-system module sdc files to Mid-end, they need to pass through the KPI system check. Problems will be detected and score at this stage will be affected. For example, if netlist has some unfriendly structure to CTS engine, it may result in more CTS buffers and longer clock latency.

For Mid-end engineers, they are required to use KPI system to check the synthesized netlist and merged sdc files. Missing clock definition, or wrong clock relationships etc. will be reported. After CTS stage, it also needs to evaluate the impact of clock paths on the timing result.

For Back-end engineers, KPI system can be used before CTS, to check physical placement of clock network, analyze clock structure, and make optimal CTS strategies; and also after CTS, to identify the bottleneck and improve the CTS quality.

With the help of KPI scores on ClockExplorer platform, we have clear pictures of clock design at each design stage. It helps to guarantee the clock design quality, and optimize chip performance eventually.

Clock KPI System for Better PPA of Complex Clock Design with ClockExplorer

Huada Empyrean Software / Spreadtrum Communications

Clock KPI System for Better PPA of Complex Clock Design with ClockExplorer

Spreadtrum/Empyrean

2017.09

Presenter: Jamie Chen

Principle Application Engineer

Empyrean

上海 • 北京 • 深圳 • 天津 • 成都 • 厦门 • 台北 • 圣迭戈 • 韩国 • 印度 • 芬兰

SPREADTRUM

Leading Mobile Communication SoC Design

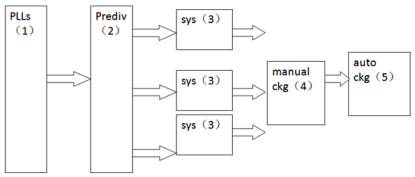
SPREADTRUM

- Process Node Trend
  - TSMC 28nm: 2G/EDGE, 3G, 4G
  - TSMC 16nm/12nm FFC: 4G
  - TSMC 10nm/7nm
- Design Trend
  - High performance
  - Low power
  - Small area

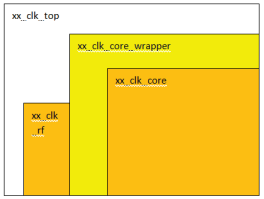
Complex Clock Network in Comm. SoC Design

SPREADTRUM

- Clock network becomes more and more complex
  - Multiple Clock Stages



  - Multiple Clock Hierarchy



  - Too many SDC files and clock definitions and exceptions
    - Third-party IP SDC files
    - Block SDC files
    - Sub system SDC files

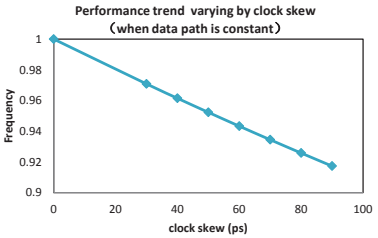
SDC statistics of a sub system

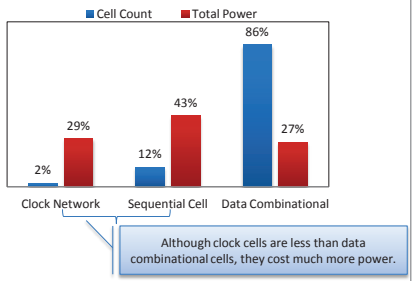
sdcCategory	Parameter	Count
General	totalLines	43412
Clock	create_clock	398
Clock	create_generated_clock	337
Clock	set_clock_group	510
Exception	SCA	762
Exception	MCP	199
Exception	SFP	92
Exception	SOD	2626
Exception	SID	2546
Exception	set_clock_sense	23
Exception	set_disable_timing	632

Clock Network Quality Effect on PPA

SPREADTRUM

- Clock network quality always have crucial effect on the Performance, Power and Area of whole chip.





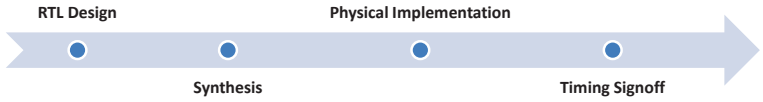
Challenges on Clock Design Process

- The clock network quality can be affected in each stage of the whole design process.
- It's difficult to locate which stage cause the problem.
  - RTL design stage (Front-end)
    - Clock structure building
    - SDC preparation

    Base of clock design quality
  - Synthesis stage (Front/Middle-end)
    - Clock gating insertion
    - SDC merging

    Key of switching power & timing constraint
  - Physical Implementation stage (Back-end)
    - CTS

    Decisive step of final clock tree quality
  - Timing Signoff stage (Front/Middle/Back-end)



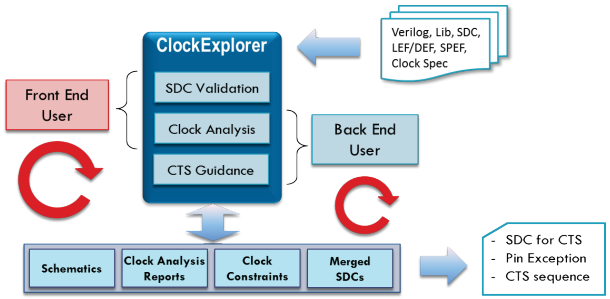
Collaboration with Empyrean

- Empyrean introduce ClockExplorer in 12/2014
- Initiated partnership in 3 phases
  - Phase I : common discussion on KPI frame construction
  - Phase II: existing clock design analysis and diagnosis
  - Phase III: customize check items for complex SoC clocks
- Goals
  - Ensure the clock design quality
  - Improve final SoC PPA

ClockExplorer Platform

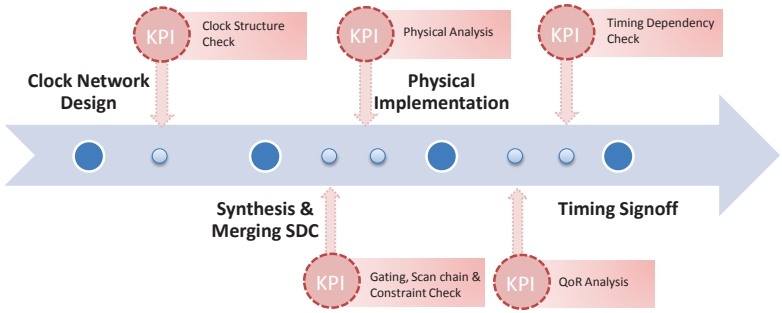
- A rule-based clock KPI system for better clock design quality

  "Certificated by TSMC OIP for N28/N16"
- A common platform for front-end & back-end to better communicate on clock design and CTS implementation.

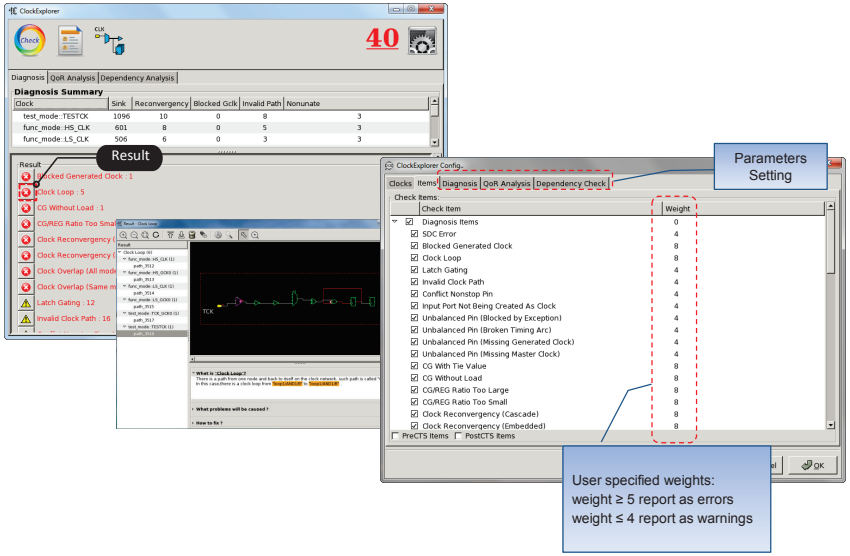


Clock KPI System Integration into Flow

- The quality of each clock design stage will be scored by KPI system according to pre-defined inspection rules.



ClockExplorer KPI System Main Window



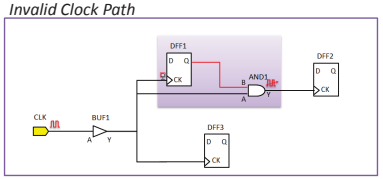
KPI Stage 1.
-- Clock Structure Check Before CTS

<Front-end>

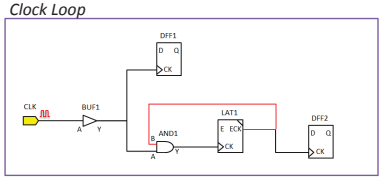
CTS Unfriendly Clock Structures

- Some unfriendly clock structures may be the source of bad CTS quality.
- The KPI system will catch those patterns and evaluate the optimization degree of original clock design.

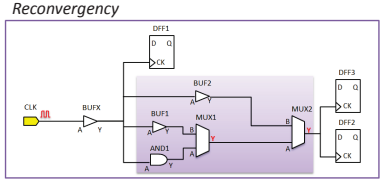
Invalid Clock Path



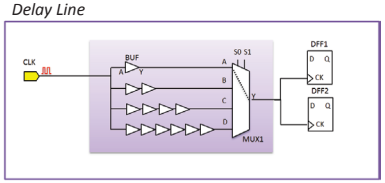
Clock Loop



Reconvergency



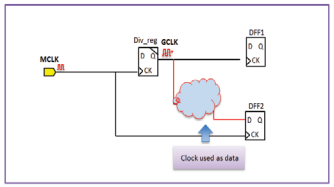
Delay Line

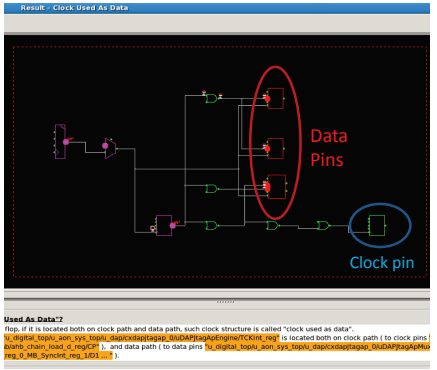


Example: Clock Used as Data

- Some divider flop is located both on clock path and data path.
- It will be difficult for some CTS tools to balance the divider flop and the flops on the clock path and data path.
- Also different the data and clock transition constraint may cause over-constrained on data path.

Clock Used as Data





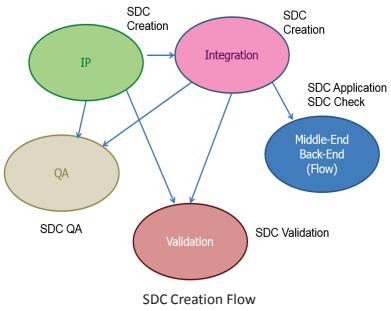
SPREADTRUM

KPI Stage 2.
-- Clock Definitions, Gating & Scan Chain Check Before CTS

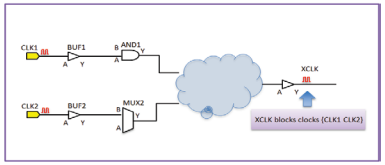
<Front-end>
<Middle-end>

Clock Definitions Check

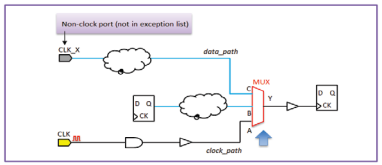
- SDC creation flow always have many iterations due to missing, wrong, or improper clock definitions.
- The KPI system will detect the potential clock definition issues and score the constraint.



Cross Clock Domain



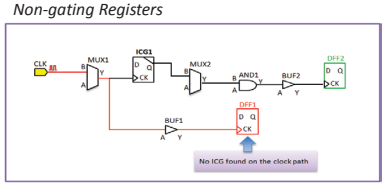
Mux With Both Clock and Data Signal



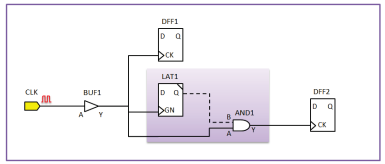
Gating Logic & Scan Chain Insertion Check

- During synthesis, the gating logic will be inserted. The coverage of clock gating will affect the switching power consumption of whole design.
- After synthesis, scan chain will be inserted. The quality of scan chain insertion will affect the scan clock timing.
- The KPI system will evaluate the optimization degree of inserted gating logic and scan chain.

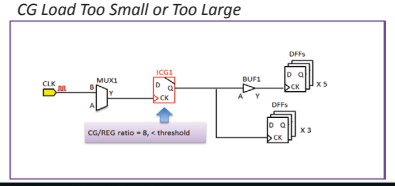
Non-gating Registers



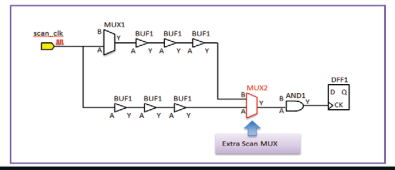
Latch Gating



CG Load Too Small or Too Large



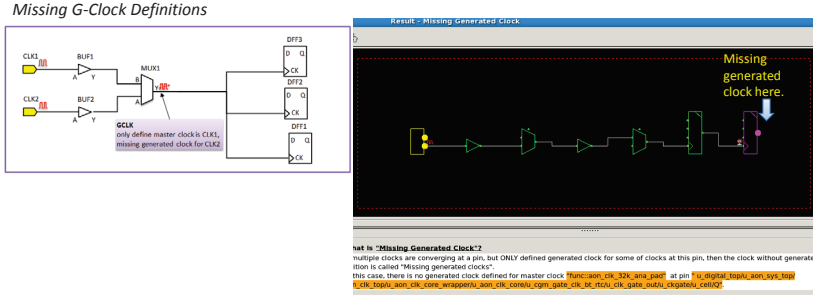
Extra Scan Mux



Example: Missing Generated Clock Definitions

- When multiple clocks are converging at a pin, if there are only generated clocks defined for part of them, those clocks without generated definitions will be blocked at this pin.
- The downstream sink pins will not be balanced on the blocked clocks.

Missing G-Clock Definitions



SDC Creation Flow

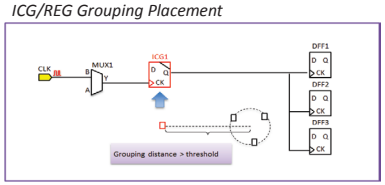
KPI Stage 3,4.
-- Physical Analysis Before CTS & QoR Analysis After CTS

<Backend>

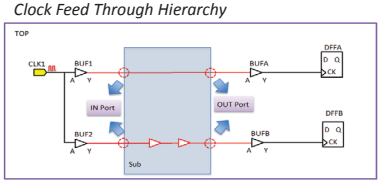
Physical Placement Analysis Before CTS

- Proper physical placement can bring beneficial effect on CTS. Improper placement may cause messy CTS results.
- The KPI system will analyze the physical bottleneck and evaluate placement quality according to user defined threshold.

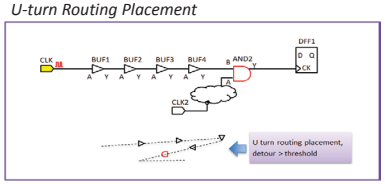
ICG/REG Grouping Placement



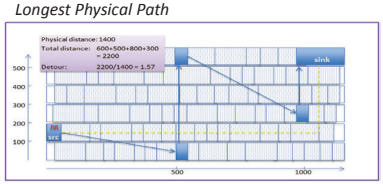
Clock Feed Through Hierarchy



U-turn Routing Placement



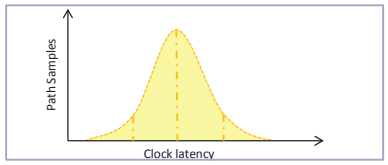
Longest Physical Path



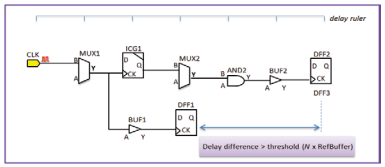
QoR Analysis After CTS

- After CTS, QoR analysis of the KPI system will be performed to evaluate CTS quality.

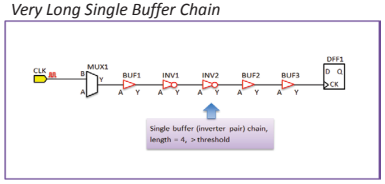
Latency Distribution



Clock Tree Length Difference Too Large



Very Long Single Buffer Chain

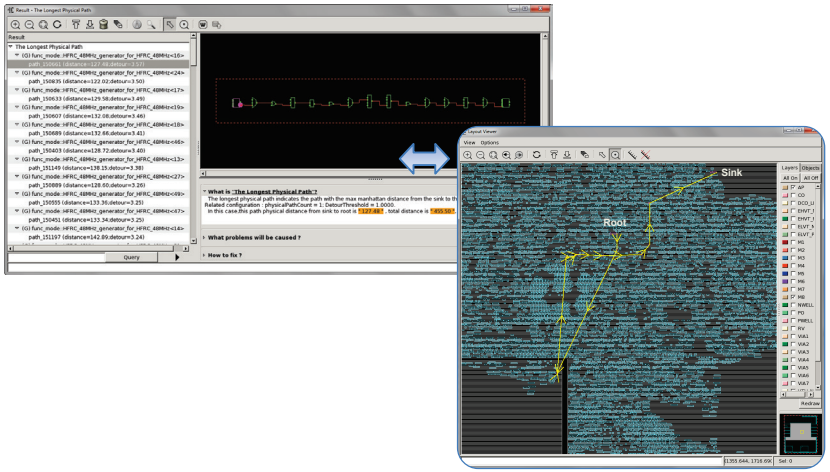


DRC Violations

- Max Transition
- Max Capacitance
- Max Fanout

Example: Longest Physical Path

- Detour of the longest physical path causes more CTS buffers and longer latency.



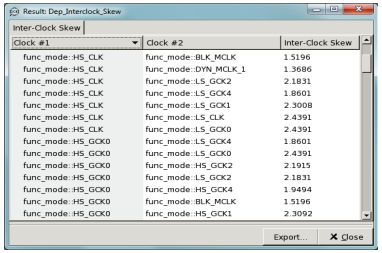
KPI Stage 5.
-- Timing Dependency Check After CTS

<Front-end>
<Middle-end>

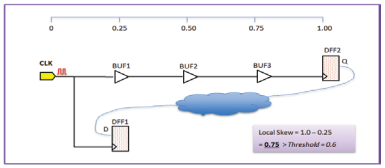
Timing Dependency Check After CTS

- Skew between clock paths with timing dependent relationship play a key role in the timing closure.
- Unreasonable skew on cell and net will cause serious OCV effect and bring difficulty to timing signoff.
- Stage 5 of KPI system will analyze those clock paths with timing talking and report those with potential risks.

Inter-Clock Skew



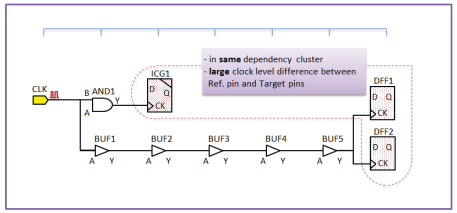
Local Skew/Local Net Skew

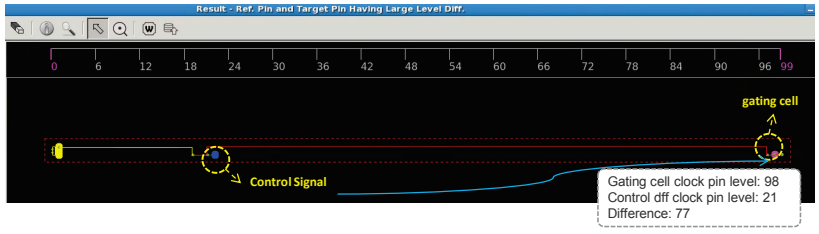


Example: Ref. Pin & Target Pin Level Difference

- The large skew between the divider and its control logic which may cause timing violations.

Ref. Pin & Target Pin Level Difference





Benefits & Success Story

- Benefits
  - Fewer backwards and forwards iterations
  - Shorter clock latency
  - Less clock power
  - Less setup violations
- Tapeout TSMC 28nmHPC+ Mobile design (15M instances)
  - Inspect clock structure & constraints
  - Modify constraints and resolve unfriendly structure
  - Analyze clock QoR and timing dependency
  - Adjust placement and CTS strategy

	CTS Buf/Inv Count	CTS Buf/Inv Area	Longest Clock Latency (ns)	SDC Creation Iteration (day)
w/o ClockExplorer	127686	735691	4.678	45
w/ ClockExplorer	**111032**	**618228**	**4.253**	**15**
Improvement	**-15%**	**-19%**	**-10%**	**-66.7%**

Summary

- Clock design quality should be controlled at each design stage: front-end, mid-end, and back-end.
- ClockExplorer helps to provide a common platform, which can view the clock structure and check the clock design.
- With the help of KPI scores, we have clear pictures of clock design at each design stage. It helps to guarantee the clock design quality, and optimize chip performance eventually.